Abridgment

Traffic-Responsive Ramp Control Through the Use of a Microcomputer

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Traffic-responsive ramp control has been proved effective in the reduction of traffic congestion on major metropolitan freeways. Equipment used at most of the existing traffic-responsive ramp-control installations involved the use of large-scale process computers and microcomputers, which are not the most cost-effective alternatives. A low-cost ramp controller is needed that can serve traffic-responsive ramp controls either for single-ramp local operations or for operations involving a series of ramp locations that link to a central computer for multilevel controls.

Since 1974, the California Department of Transportation has been conducting researches and evaluations on the application of microcomputer for traffic-responsive ramp controls. The department found that recent advancements in the large-scale integration metal oxide semiconductor technology have made possible many applications for microcomputers. The second-generation microcomputers have sufficient capabilities to replace large-scale computers and minicomputers in most traffic control functions. The attractive features of microcomputers include low cost, small physical size, and operability within the ambient temperature range of -18°C to 60°C (-27.78°F to 15.56°F) without air conditioning. The physical size of a typical microcomputer chip is approximately 51 by 16 by 4 cm (2 by 0.6 by 0.15 in), and a read-only-memory chip with 1024 by 8 bits of storage capacity is approximately 28 by 10 by 2 cm (1.1 by 0.4 by 0.1 in). A simple set of microcomputer chips can now be bought for less than $100.

The California Department of Transportation awarded the first contract to Honeywell, Inc. for the manufacture of 200 Type 140 Controllers based on a design developed by the department. The Type 140 Controllers employ a Motorola M6800 microprocessor chip, 2048 by 8 bits of programmable read-only-memory (PROM) and 1024 by 8 bits of complimentary metal oxide semiconductor (CMOS) random access memory (RAM). The M6800 microprocessor can address up to 65 000 by 8 bits of memory and input-output locations. Instructions set includes functions for data transfers between working registers and with memory locations; logical and arithmetic computations on contents of working registers; increment, document, and rotate working registers; conditional and unconditional branchings; and input and output of data from and to peripheral devices. The minimum instruction execution time is approximately 2 μs. The PROM chips are manufactured by Intel by means of the silicon gate process. Each of the Intel 2708 PROM chips can store 1024 by 8 bits of information and is field programmable and erasable. The CMOS RAM is used for temporary storage of traffic data and calculation results. Backup battery power is provided in the controller to prevent loosing of the RAM content in the event of commercial power failure.

Ramp-control strategies and programs are presently being developed by the State. The Type 140 controllers are currently being used in the Los Angeles, San Diego, and San Francisco areas for local and multilevel ramp-control operations. Use of the microcomputer probably will become standard on California highways for both ramp and intersection controls, especially as a result of the growing emphasis on upgrading the operation of existing facilities rather than the building of new facilities.